In Application Serial No. 10/020,426
Filed December 7, 2001

DECLARATION OF GEORGE BENDAK UNDER 37 CFR §1.132

I, George Bendak, hereby declare as follows:

1. My residence address is 7712 Cedar Lake Ave. San Diego, CA 92119.

2. My degrees include: BS Electrical and Computer Engineering

MS Electrical and Computer Engineering with emphasis in communications and signal processing.

3. A list of some of my publications is enclosed as separate attachment.

4. From 1993 until 1999, I worked at ComStream Corporation in San Diego, with the Research and Development Department designing satellite communication products for both commercial and military use.

5. Since 1999 I have been employed by Applied Micro Circuits Corp. (AMCC), 6290 Sequence Drive, San Diego, CA 92121. My title at AMCC is Solutions Architect. My responsibilities include identifying the needs of potential customers and architecting system solutions for them. This includes researching and writing IC specifications. The ICs I work on range from serial tx/rx communication devices, to FEC devices, network processing and traffic management devices, and to terabit class protocol-agnostic switch fabric systems.

6. I have read claims 17, 33, and 35 of the patent application entitled SYSTEM AND METHOD FOR NON-CAUSAL CHANNEL EQUALIZATION, Castagnozzi et al., Serial Number 10/020,426 (the Applicant). I have read the Office Action dated July 13, 2005, concerning the rejection of 33 as anticipated by Andresen (US 3,670,304), the rejection of claim 17 as obvious with respect to Andresen and the definition of non-return-to zero (NRZ), and the rejection of claim 35 as obvious with reject to Andresen, the definition, and Abe (US 5,781,588).

7. I have read the Applicant's description of the Andresen invention in the accompanying response, and I find that description accurate. I have also read the description of the Andresen invention in the Office Action dated July 13, and I find that explanation inaccurate in a number of respects. The Applicant's response addresses these inaccuracies on a point-by-point basis. Again, I find the Applicant's point-by-point rebuttal of the assertions in the Office Action to be accurate, so I see no need to repeat those arguments in this paper. Rather, I will attempt to compare the Andresen patent to the Applicant's claims from a top-level perspective.

The basic components of the Applicants claims are a multi-threshold circuit and a non-causal circuit. The multi-threshold circuit provides a "plurality of bit estimates" for each input signal. As seen in Figs. 7A and 7B, in one implementation, the bit estimates are a measurement of the input signal that is responsive to three different threshold levels. Andresen describes a composite threshold circuit with a feedback adjustment mechanism. However, Andresen does not describe a circuit that provides a plurality of bit estimates for each input data, as recited in Applicant's claims 17, 33, and 35. Andresen provides a single "estimate" for each input signal.

In my opinion, Andresen does not describe the Applicant's multi-threshold circuit.

The Office Action appears to confuse the Applicant's non-causal circuit with a conventional feedback mechanism for adjusting a threshold. This is actually a compound error because it incorrectly merges the functions of the multi-threshold circuit with the non-causal circuit, and because it fails to appreciate the significance of the non-causal analysis being performed. First, even if the thresholds of the multi-threshold are adjusted using feedback, such as the FEC analysis recited in claim 35, this adjustment has nothing to do with the non-causal analysis of bit decisions made across several clock periods.

Second, the non-causal circuit is not an analog feedback circuit. In a sense, it includes a "digital feedback" component, but even this explanation misses the mark. The circuit compares bit decisions of different clock periods. I am aware of conventional circuitry that integrates voltage signals (using "past" analog information) in the calculation a current clock bit decision. However, I am unaware of any conventional circuits that use past (digital) decisions in the calculation of a current clock decision. This factor, by itself, makes the Applicant's claims novel. However, the non-causal circuit goes a step further and uses both past and "future" digital decisions in the calculation of the present bit decision. Again, I find this factor completely unique in the art.

One further aspect of novelty can be appreciated by combining the function of the mutli-threshold circuit with the non-causal circuit. The multi-threshold circuit provides a multi-threshold estimate of each input signal. The invention "works" because it is able to interpret the multi-threshold input, in light of previous and future decisions, to make the best

decision in the current clock cycle. Again, I find the conversion of a multi-threshold analog signal into a digital signal, based upon the decisions made in adjacent clock periods, to be absolutely unique.

In summary, I don't find any similarities between Andresen and claim 33 (or 17, or 35). I do not understand why Andresen is being used as a prior art reference because it does not describe even a single function of the Applicant's claims. Andresen does not provide a plurality of bit estimates for each input data. Andresen does not compare a plurality of bit estimates for a current clock cycle, to bit decisions made in previous and subsequent clock cycles, for the purpose of making a bit decision for a current clock.

8. Regarding the rejection of claim 17 as obvious, I do not find it implausible that Andresen's tape read system could be adapted to use the NRZ format. However, I do not understand how an expert could be expected to perform such a modification using a dictionary definition. Further, such a modification to Andresen is irrelevant. It is irrelevant because even if Andresen was modified to work in the NRZ format, that modification could not perform the functions of the claimed invention. Andresen, as modified, would still not provide a plurality of bit estimates for each input data. Even modified, Andresen could not compare a plurality of bit estimates for a current clock cycle, to bit decisions made in previous and subsequent clock cycles, for the purpose of making a bit decision for a current clock, as recited in claim 17.

9. I do not find that the combination of Andresen, the dictionary definition, and Abe make claim 35 obvious. The Abe reference has apparently been cited to introduce the subject matter of a threshold adjustment mechanism that is based upon the analysis of BER data - the Office Action describes the circuit of Fig. 37 in particular. It may be possible

to modify Andresen, to use BER analysis to adjust thresholds. However, it is not apparent to me how Andresen's feedback circuitry could be modified to perform such a task.

However, once again I find such an analysis beside the point. Even if Andresen was modified to work in the NRZ format, using BER data to adjust thresholds, that modification could not perform the functions of the claimed invention. Andresen, as modified, would still not provide a plurality of bit estimates for each input data. Neither could the modified Andresen device compare a plurality of bit estimates for a current clock cycle, to bit decisions made in previous and subsequent clock cycles, for the purpose of making a bit decision for a current clock, as recited in claim 35.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United State Code and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

Aug. 4, 2005 George Bendak

Date George Bendak